**Chapter 6: TIMING DIAGRAM**

**Topic – 1: Introductory Concepts**

**Introduction**

* Is used to **track the changes** occurring in the microprocessor.
* Like changes and variations in the **status of signals**.
* **Vertical axis** represents **various signals** & if they are **high** or **low**.
* It is generally used to represent **how** an instruction executes.

**Common Terminologies**

* **T state:** An operation carried out during **one** time period.
* **Instruction cycle:** Time required to **fetch** **& execute** an instruction.
* **Fetch cycle:** Process of **reading an instruction** to be executed from memory.
* Each instruction of a program is first converted to **hex** code & then to **binary** before being **stored** at some part of the memory.
* **Execution cycle:** Process of **executing** the fetched instruction.
* **Machine cycle:** Time required to **access a memory or I/O** device for **read** or **write** operation.

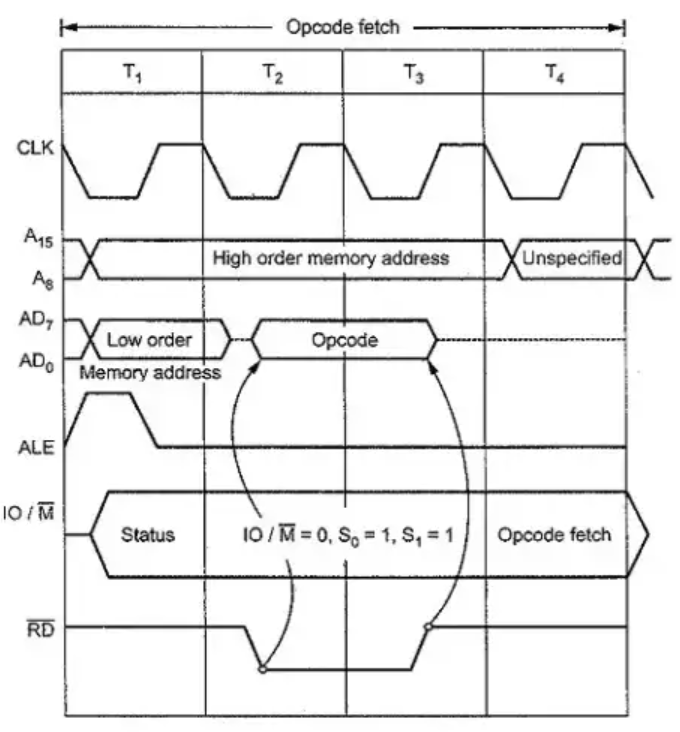
**Topic – 2: Machine Cycle**

**Control Signals in Timing Diagram**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sno.** | **Machine Cycle** | **IO/M** | **S1S0** | **Other Control Signals** |
| **1** | **Opcode fetch machine cycle** | **0** | **11** | **RD = 0** |
| **2** | **Memory read machine cycle/ operand fetch machine cycle** | **0** | **10** | **RD = 0** |
| **3** | **Memory write machine cycle** | **0** | **01** | **WR = 0** |
| **4** | **IO read machine cycle** | **1** | **10** | **RD = 0** |
| **5** | **IO write machine cycle** | **1** | **01** | **WR = 0** |
| **6** | **Interrupt acknowledgement machine cycle** | **1** | **11** | **INTA = 0** |
| **7** | **Bus idle machine cycle** | **0** | **00** | **INTA = RD = WR = 1** |

**Opcode Fetch Machine Cycle (OFMC)**

* It is **not** only **fetching the opcode** of the instruction, but also **decoding** it.



**1st T State**

* The **opcode address** is stored at **PC**.
* Opcode’s **higher** & **lower** bits are extracted by **bus pins**.
* Opcode bits are **demultiplexed**.
* **ALE** pin is activated to show that **AD0 – AD7** contain **lower address bits**.
* **IO/M** signal is **low** at beginning, meaning that **opcode** will be fetched from memory.
* **S0** and **S1** are **1** to show its OFMC.

**2nd T State**

* **ALE** signal goes **low**.
* **Lower address bits** are latched.
* **AD0 – AD7** is **free** to be used as **data bus**.
* **RD** goes **low**, as reading process starts & opcode is fetched to **AD0 – AD7**.
* **Higher bits** are still present in **A8 – A15**.

**3rd T State**

* Opcode stays on **data bus** until mid of **3rd T state**.
* **RD** goes **high** & opcode is placed on **IR**.

**4th T State**

* Opcode is **decoded**.
* ***MOV*** instructions are completed in **4th T state** itself.
* Microprocessor decides to continue more **T state cycles** or **not**.
* **PC** is always **incremented** by **1** on last **T state**.

**5th & 6th T State**

* Some instructions might take **6 T states**.
* Examples of instructions coming under **OFMC** are **DCX**, **INX**, **PCHL**, **SPHL**, **CALL**, **RSTN** & conditional **RET**.